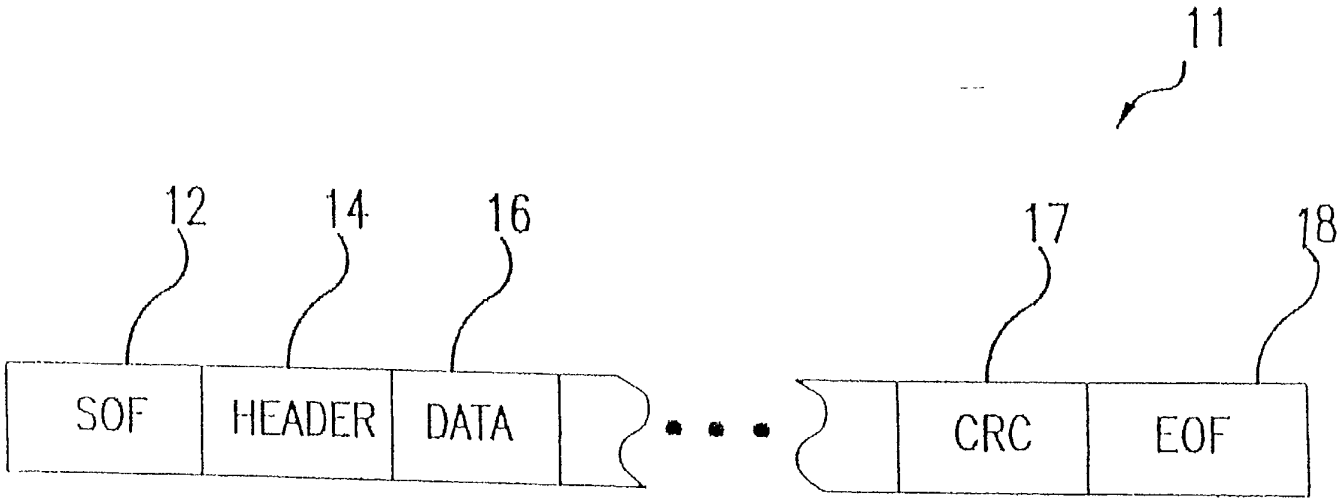

FIG. 1A

PRIOR ART

T02207 "E9827860

14

Routing Control (R_CTRL)	Destination ID (D_ID)	
Class Specific Control (CS_CTL)	Source ID (S_ID)	
Data Structure Type (TYPE)	Frame Control (F_CTL)	
Sequence ID (SEQ_ID)	Data Field Control (DF_CTL)	Sequence Count (SEQ_CNT)
Originator ID (OX_ID)		Responder ID (RX_ID)
Parameter or Relative Offset		

FIG. 1B
PRIOR ART

T02207 "E982860

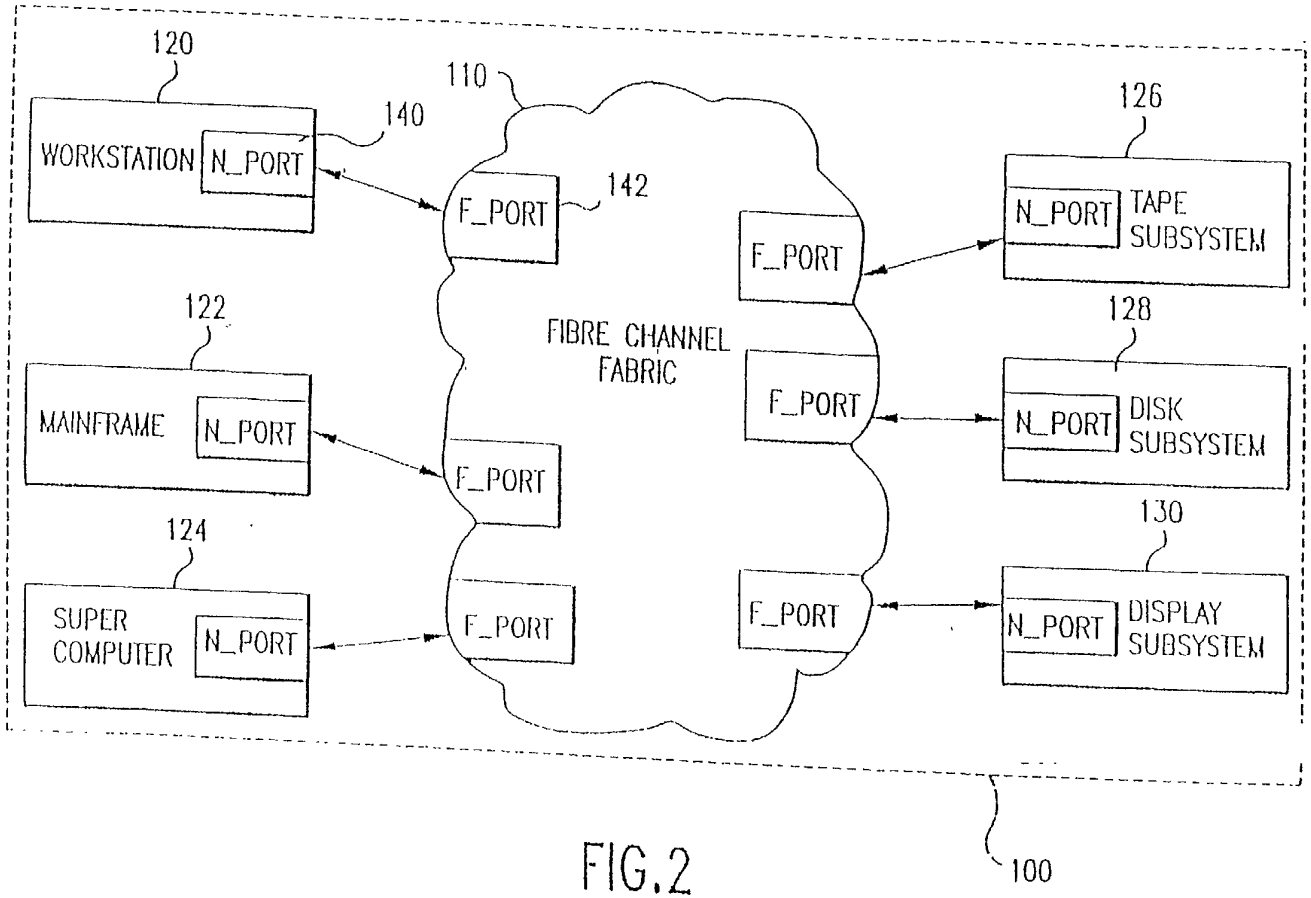

FIG.2
PRIOR ART

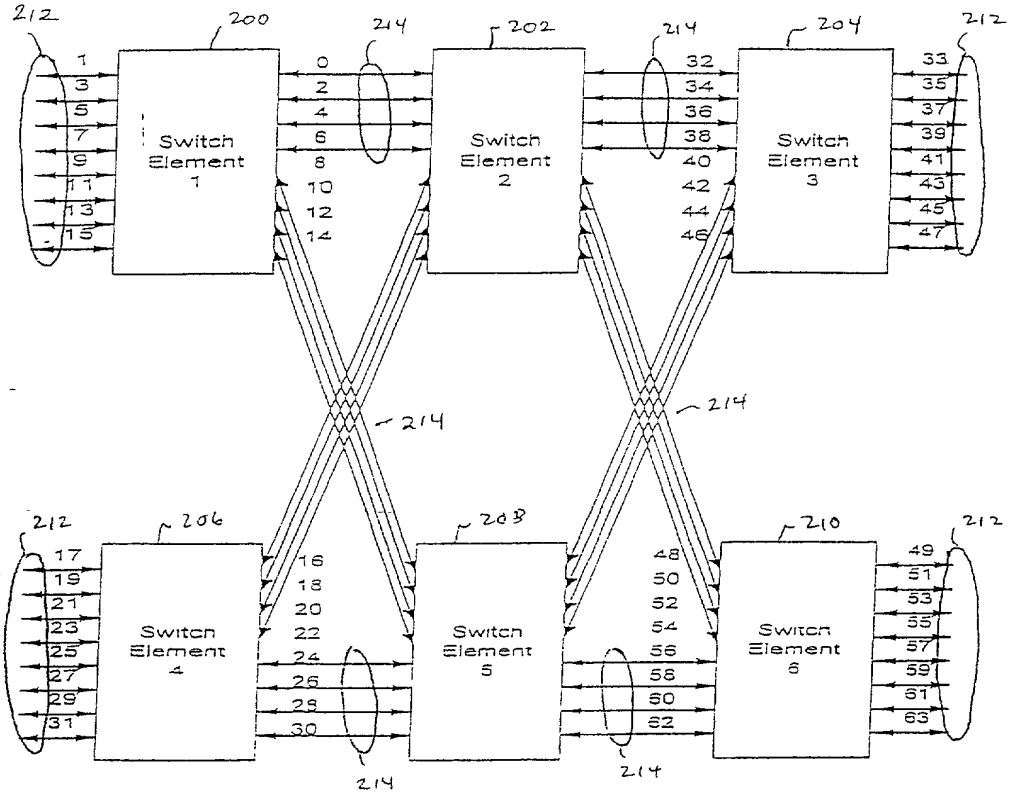
212
200
214
202
214
204
212
Switch Element 1
Switch Element 2
Switch Element 3
214
214
212
206
208
210
212
Switch Element 4
Switch Element 5
Switch Element 6
214
214

FIG. 3

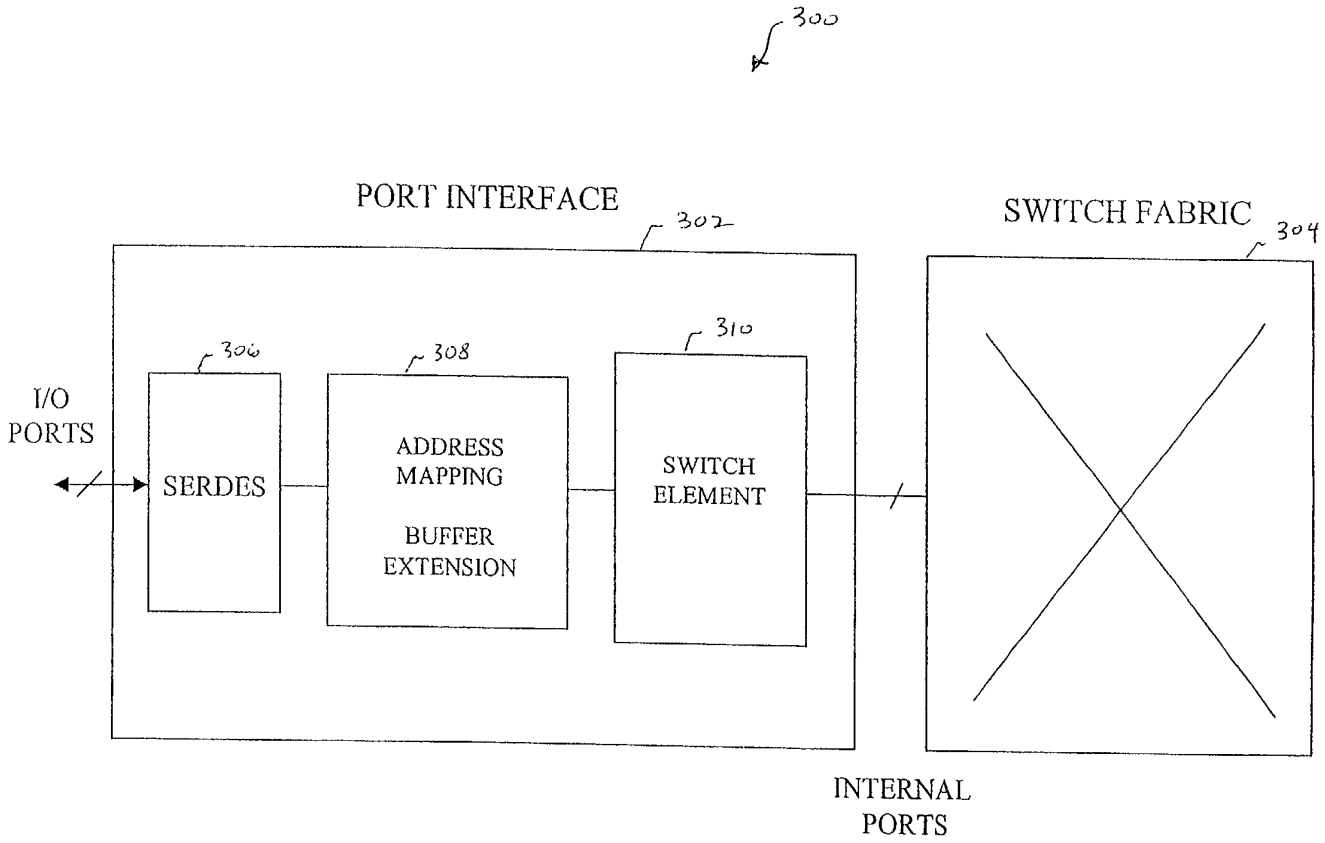
300
PORT INTERFACE
302
SWITCH FABRIC
304
306
308
310
I/O
PORTS
SERDES
ADDRESS
MAPPING
BUFFER
EXTENSION
SWITCH
ELEMENT
INTERNAL
PORTS

FIG. 4

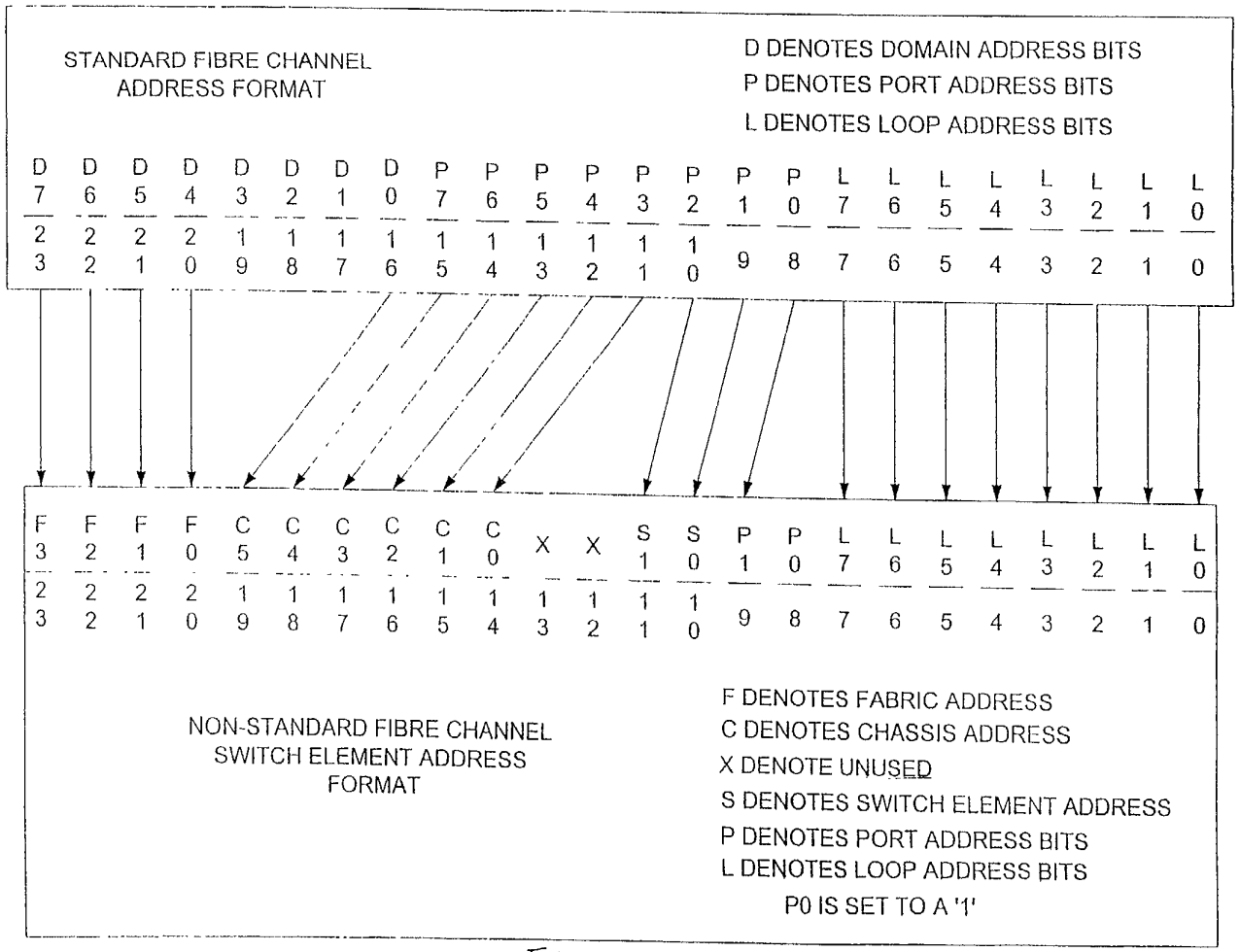
STANDARD FIBRE CHANNEL
ADDRESS FORMAT
D DENOTES DOMAIN ADDRESS BITS
P DENOTES PORT ADDRESS BITS
L DENOTES LOOP ADDRESS BITS
D7 D6 D5 D4 D3 D2 D1 D0 P7 P6 P5 P4 P3 P2 P1 P0 L7 L6 L5 L4 L3 L2 L1 L0
23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
F3 F2 F1 F0 C5 C4 C3 C2 C1 C0 X X S1 S0 P1 P0 L7 L6 L5 L4 L3 L2 L1 L0
23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
NON-STANDARD FIBRE CHANNEL
SWITCH ELEMENT ADDRESS
FORMAT
F DENOTES FABRIC ADDRESS
C DENOTES CHASSIS ADDRESS
X DENOTE UNUSED
S DENOTES SWITCH ELEMENT ADDRESS
P DENOTES PORT ADDRESS BITS
L DENOTES LOOP ADDRESS BITS
P0 IS SET TO A '1'

FIG. 5A

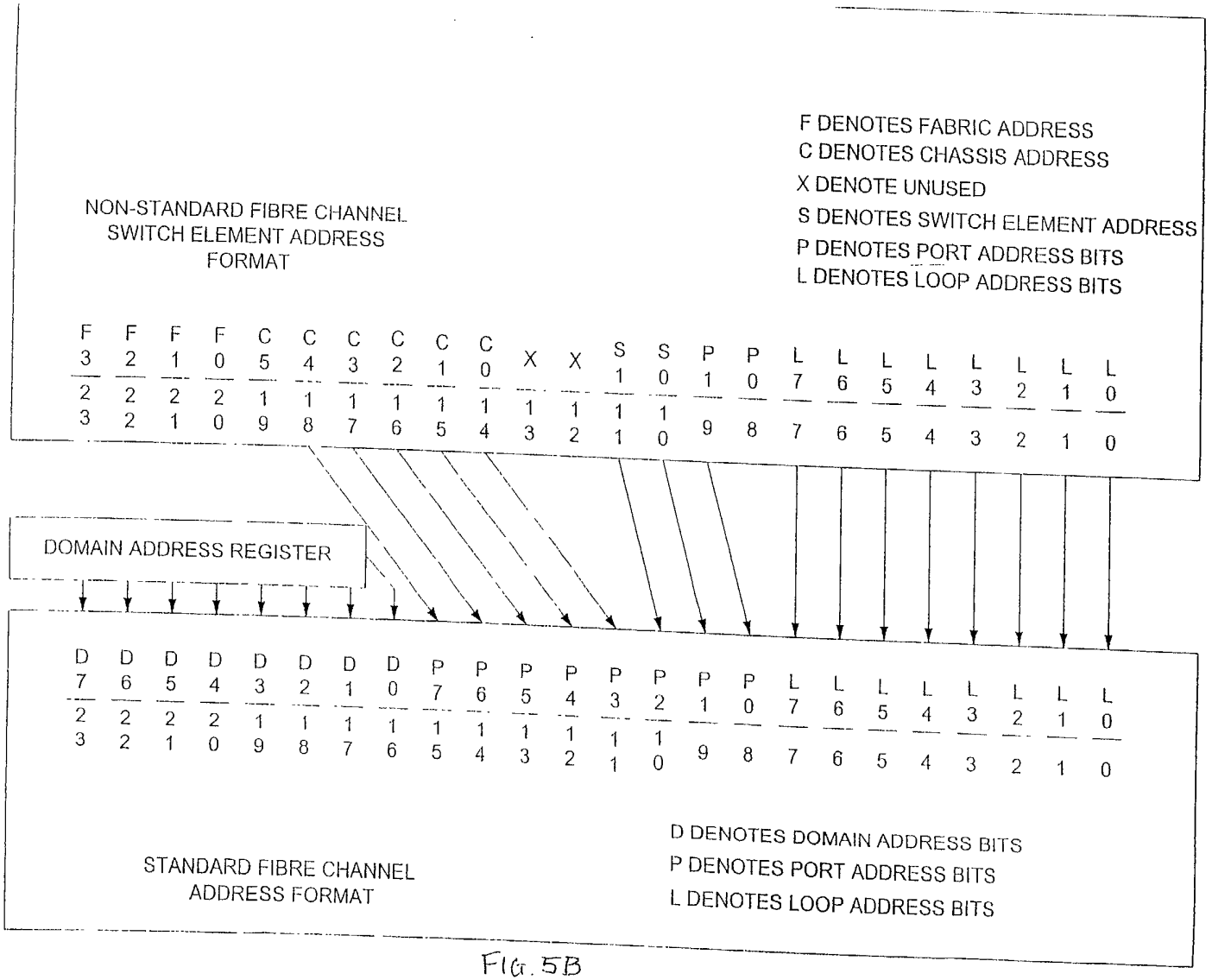
F DENOTES FABRIC ADDRESS
C DENOTES CHASSIS ADDRESS
X DENOTE UNUSED
S DENOTES SWITCH ELEMENT ADDRESS
P DENOTES PORT ADDRESS BITS
L DENOTES LOOP ADDRESS BITS
NON-STANDARD FIBRE CHANNEL SWITCH ELEMENT ADDRESS FORMAT
F F F F C C C C C C X X S S P P L L L L L L
3 2 1 0 5 4 3 2 1 0 1 0 1 0 1 0 7 6 5 4 3 2 1 0
23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
DOMAIN ADDRESS REGISTER
D D D D D D D D P P P P P P P P L L L L L L L L
7 6 5 4 3 2 1 0 7 6 5 4 3 2 1 0 7 6 5 4 3 2 1 0
23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
STANDARD FIBRE CHANNEL ADDRESS FORMAT
D DENOTES DOMAIN ADDRESS BITS
P DENOTES PORT ADDRESS BITS
L DENOTES LOOP ADDRESS BITS

FIG. 5B

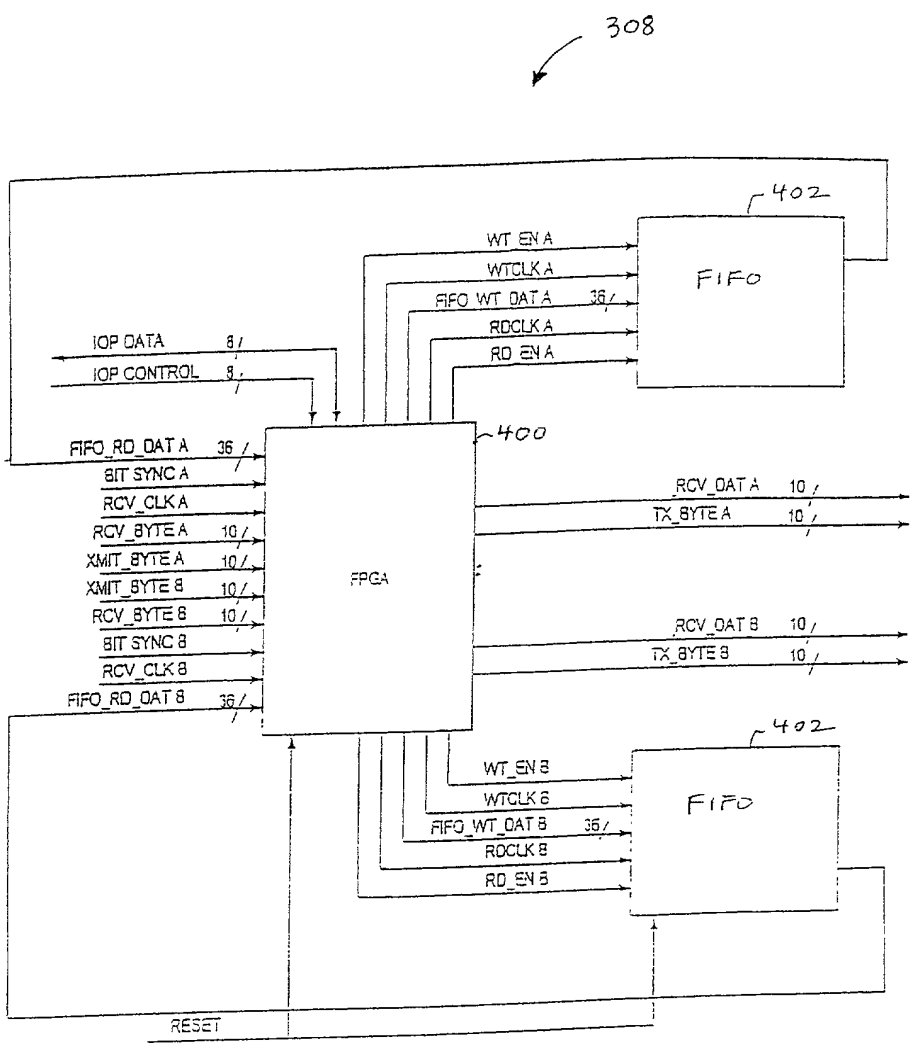
308
402
FIFO
WT_EN A
WTCLK A
FIFO_WT_DAT A
36
RDCLK A
RD_EN A
IOP DATA
8
IOP CONTROL
8
400
FIFO_RD_DAT A
36
BIT SYNC A
RCV_CLK A
RCV_BYTE A
10
XMIT_BYTE A
10
XMIT_BYTE B
10
RCV_BYTE B
10
BIT SYNC B
RCV_CLK B
FIFO_RD_DAT B
36
FPGA
RCV_DAT A
10
TX_BYTE A
10
RCV_DAT B
10
TX_BYTE B
10
402
FIFO
WT_EN B
WTCLK B
FIFO_WT_DAT B
36
RDCLK B
RD_EN B
RESET

FIG. 6

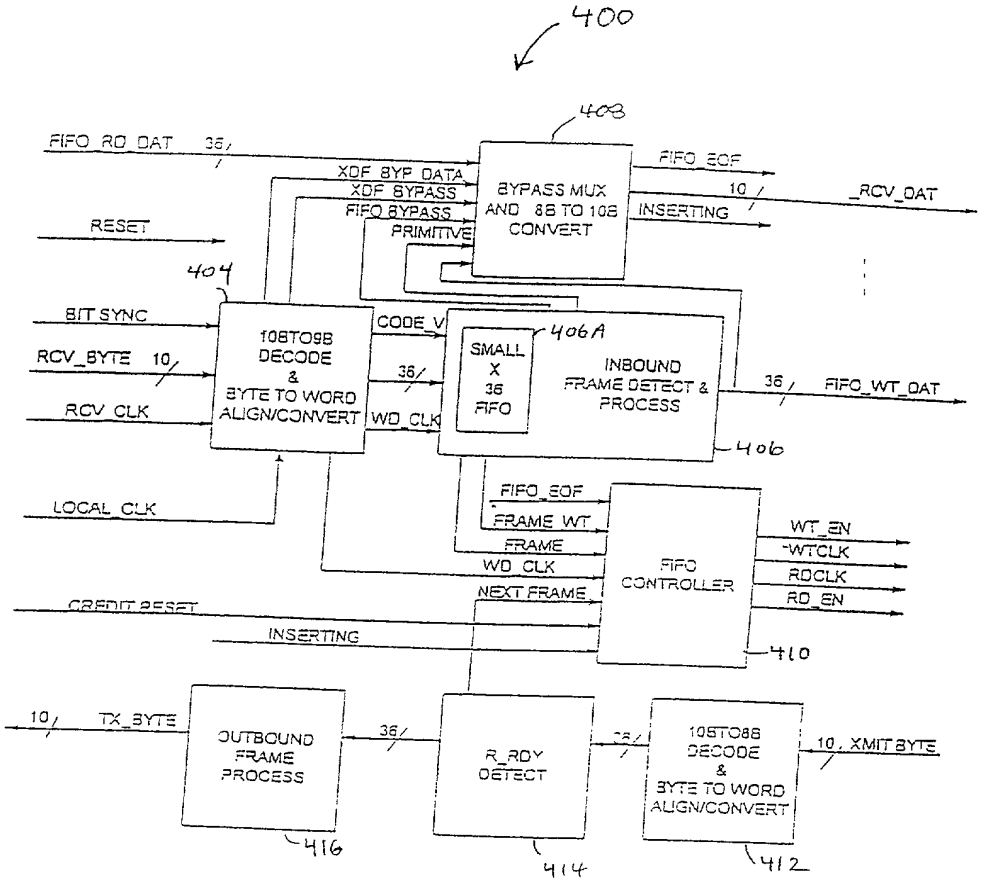
400
408
FIFO_RD_DAT
36
XDF_BYP_DATA
XDF_BYPASS
FIFO_BYPASS
PRIMITIVE
BYPASS MUX AND 8B TO 10B CONVERT
FIFO_EOF
10
_RCV_DAT
INSERTING
RESET
404
BIT SYNC
RCV_BYTE 10
RCV_CLK
10BTO9B DECODE & BYTE TO WORD ALIGN/CONVERT
CODE_V
36
WD_CLK
SMALL X 36 FIFO
406A
INBOUND FRAME DETECT & PROCESS
36
FIFO_WT_DAT
406
LOCAL_CLK
FIFO_EOF
FRAME_WT
FRAME
WD_CLK
NEXT FRAME
CREDIT RESET
INSERTING
FIFO CONTROLLER
WT_EN
WTCLK
RDCLK
RD_EN
410
10
TX_BYTE
OUTBOUND FRAME PROCESS
36
R_RDY DETECT
10STO8B DECODE & BYTE TO WORD ALIGN/CONVERT
10
XMIT BYTE
416
414
412

FIG. 7

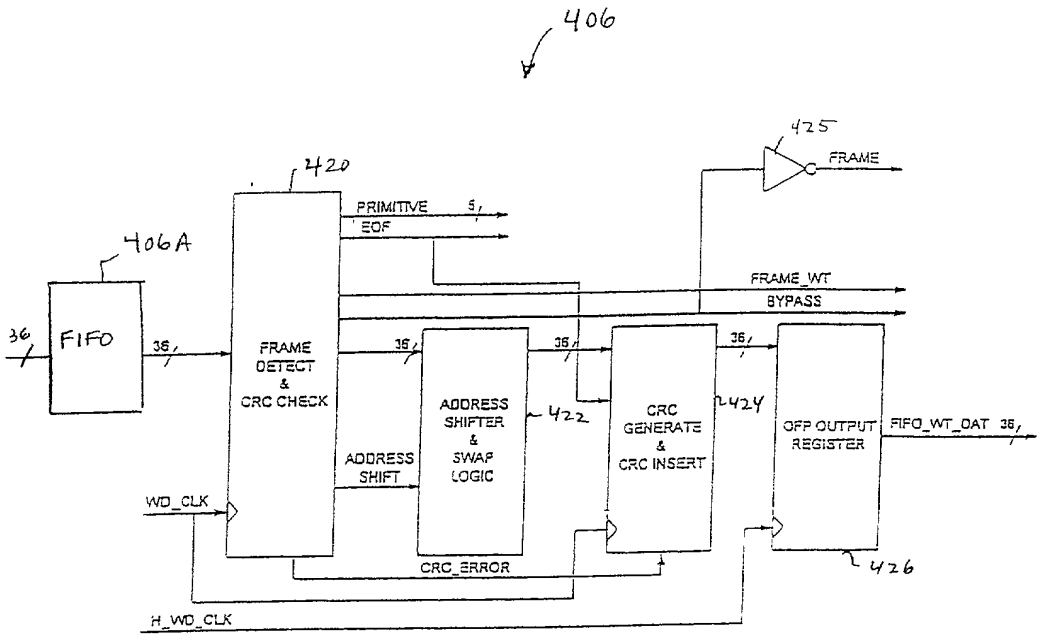
406
425
FRAME
420
PRIMITIVE
5
EOF
406A
FRAME_WT
BYPASS
36
FIFO
36
FRAME DETECT & CRC CHECK
36
36
36
36
ADDRESS SHIFTER & SWAP LOGIC
422
CRC GENERATE & CRC INSERT
424
OFP OUTPUT REGISTER
FIFO_WT_DAT
36
ADDRESS SHIFT
WD_CLK
CRC_ERROR
426
H_WD_CLK

FIG. 8

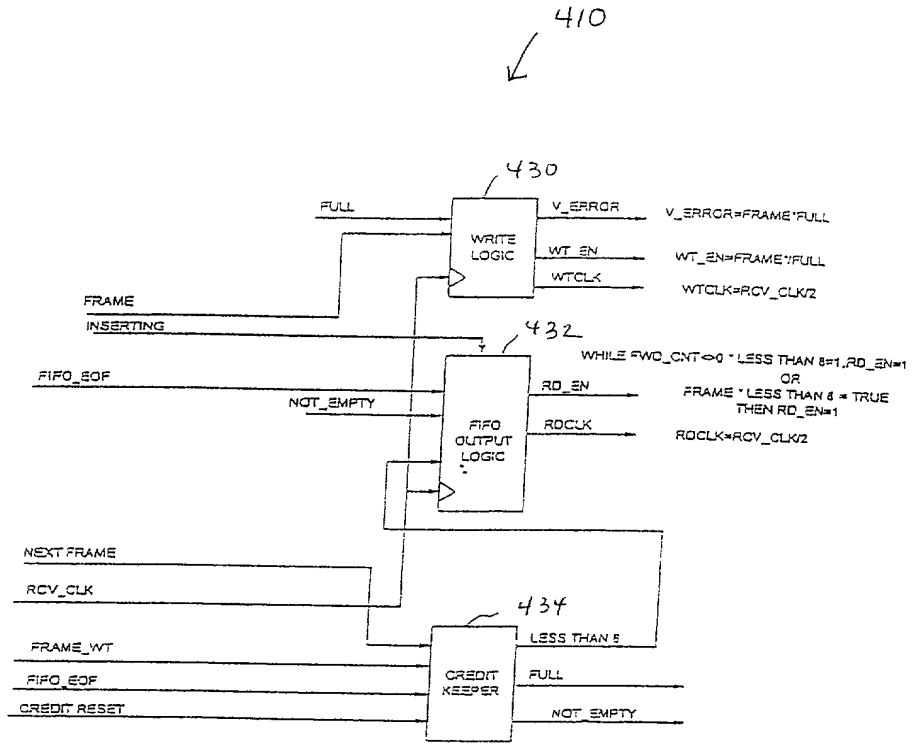
410
430
FULL
WRITE LOGIC
V_ERROR
V_ERROR=FRAME*FULL
WT_EN
WT_EN=FRAME*!FULL
WTCLK
WTCLK=RCV_CLK/2
FRAME
INSERTING
432
WHILE FWD_CNT<>0 * LESS THAN 8=1,RD_EN=1
OR
FRAME * LESS THAN 6 = TRUE
THEN RD_EN=1
FIFO_EOF
NOT_EMPTY
FIFO OUTPUT LOGIC
RD_EN
RDCLK
RDCLK=RCV_CLK/2
NEXT FRAME
RCV_CLK
434
LESS THAN 5
FRAME_WT
FIFO_EOF
CREDIT RESET
CREDIT KEEPER
FULL
NOT_EMPTY

FIG. 9

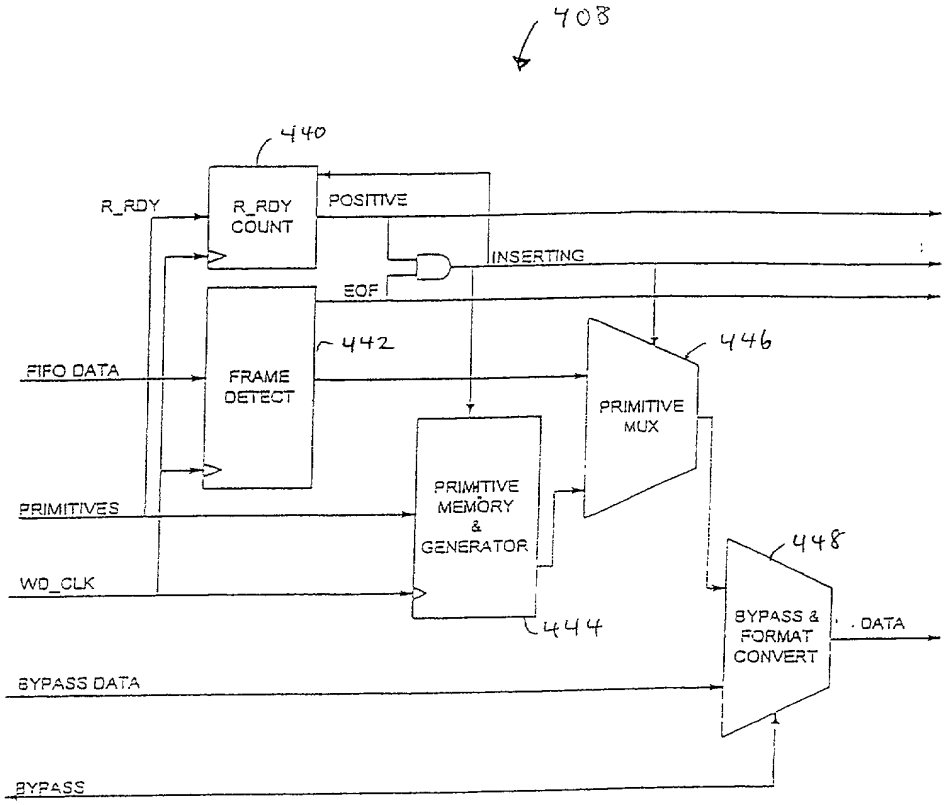
408
440
R_RDY
R_RDY COUNT
POSITIVE
INSERTING
EOF
442
FIFO DATA
FRAME DETECT
446
PRIMITIVE MUX
PRIMITIVES
PRIMITIVE MEMORY & GENERATOR
448
WD_CLK
444
BYPASS & FORMAT CONVERT
DATA
BYPASS DATA
BYPASS

FIG. 10

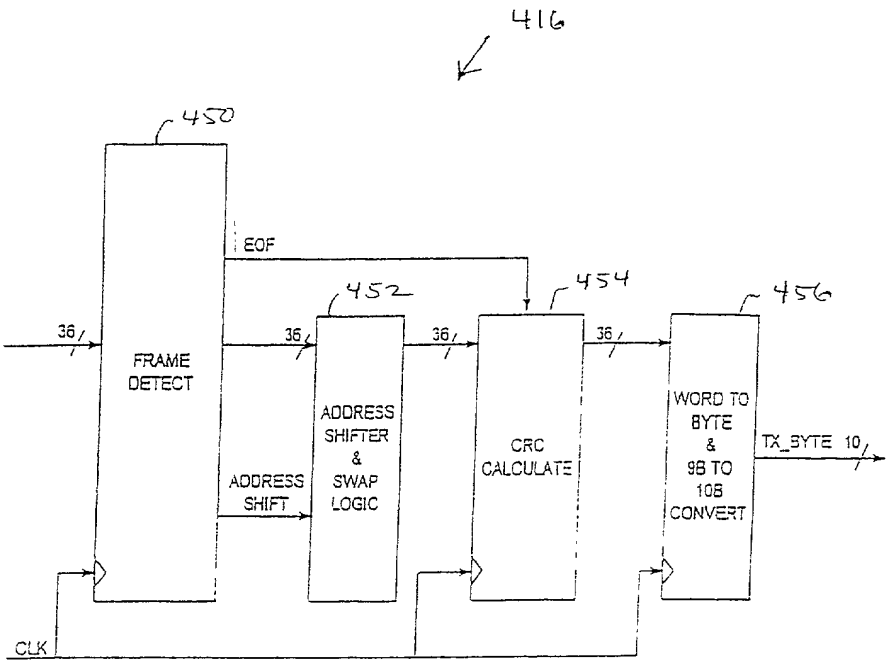
416
450
452
454
456
36
FRAME DETECT
EOF
ADDRESS SHIFT
ADDRESS SHIFTER & SWAP LOGIC
CRC CALCULATE
WORD TO BYTE & 9B TO 10B CONVERT
TX_BYTE 10
CLK

FIG. 11

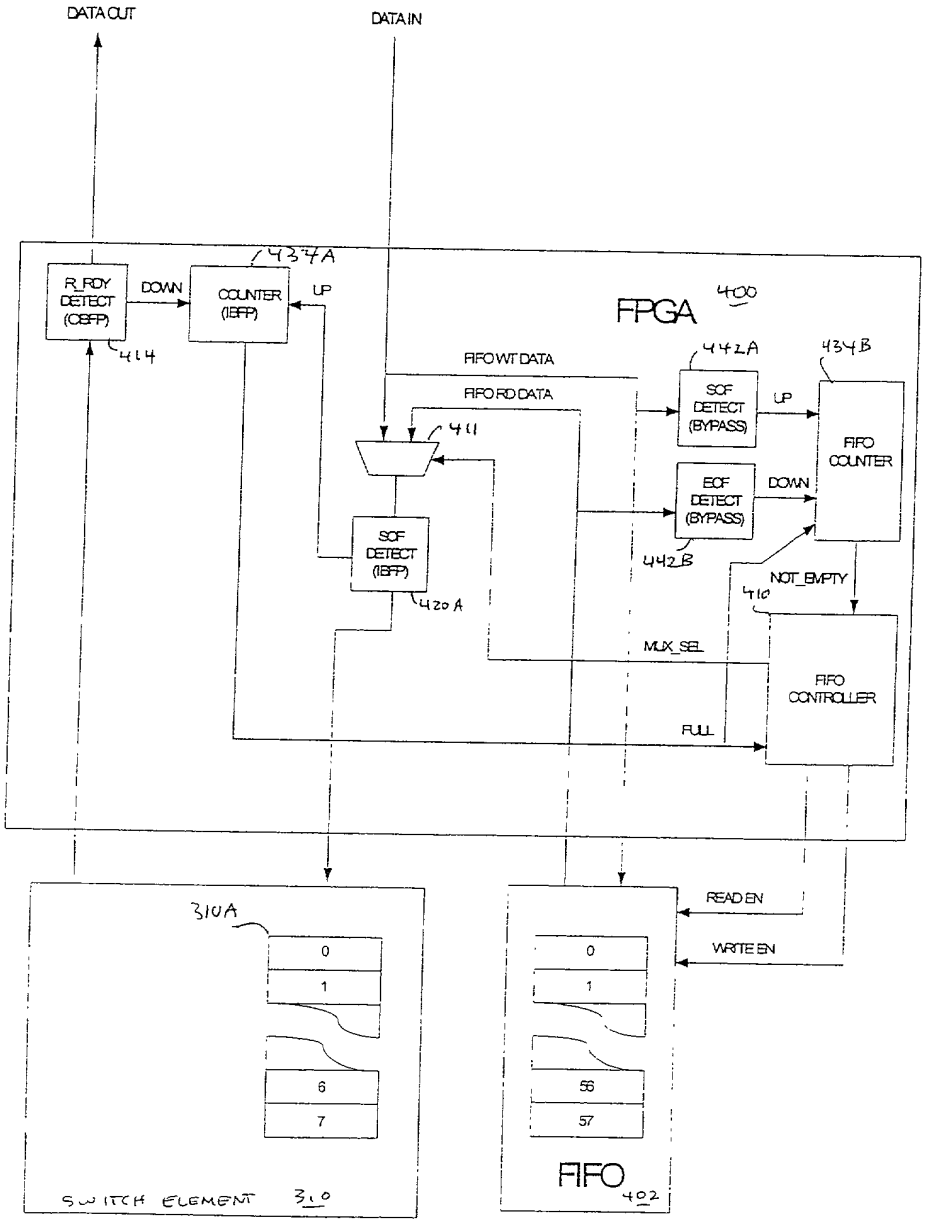
DATA OUT
DATA IN
R_RDY DETECT (OBFP)
DOWN
COUNTER (IBFP)
UP
434A
414
FPGA
400
FIFO WT DATA
FIFO RD DATA
411
SOF DETECT (IBFP)
420A
442A
SOF DETECT (BYPASS)
UP
434B
FIFO COUNTER
EOF DETECT (BYPASS)
DOWN
442B
NOT_EMPTY
410
MUX_SEL
FIFO CONTROLLER
FULL
310A
0
1
6
7
SWITCH ELEMENT 310
READ EN
WRITE EN
0
1
56
57
FIFO 402

FIG. 12

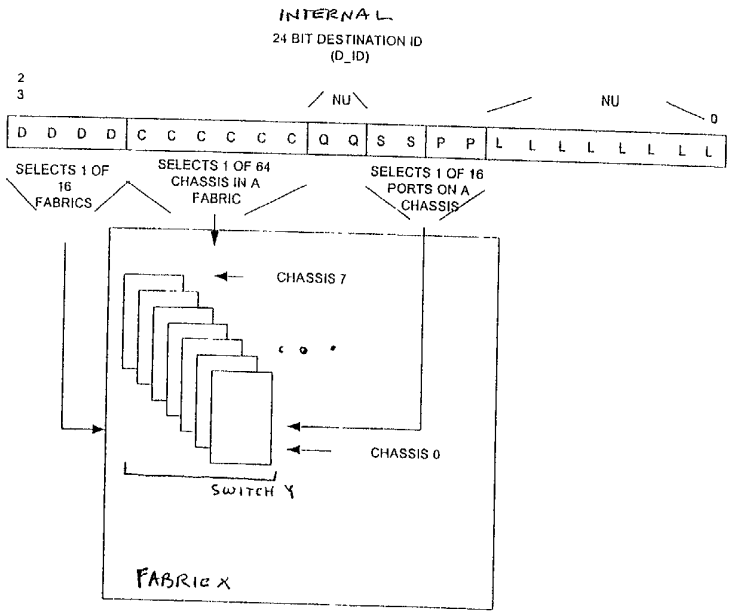
INTERNAL
24 BIT DESTINATION ID
(D_ID)
2
3
NU
NU
0
D D D D C C C C C C Q Q S S P P L L L L L L L L
SELECTS 1 OF 16 FABRICS
SELECTS 1 OF 64 CHASSIS IN A FABRIC
SELECTS 1 OF 16 PORTS ON A CHASSIS
CHASSIS 7
CHASSIS 0
SWITCH Y
FABRIC X

FIG. 13

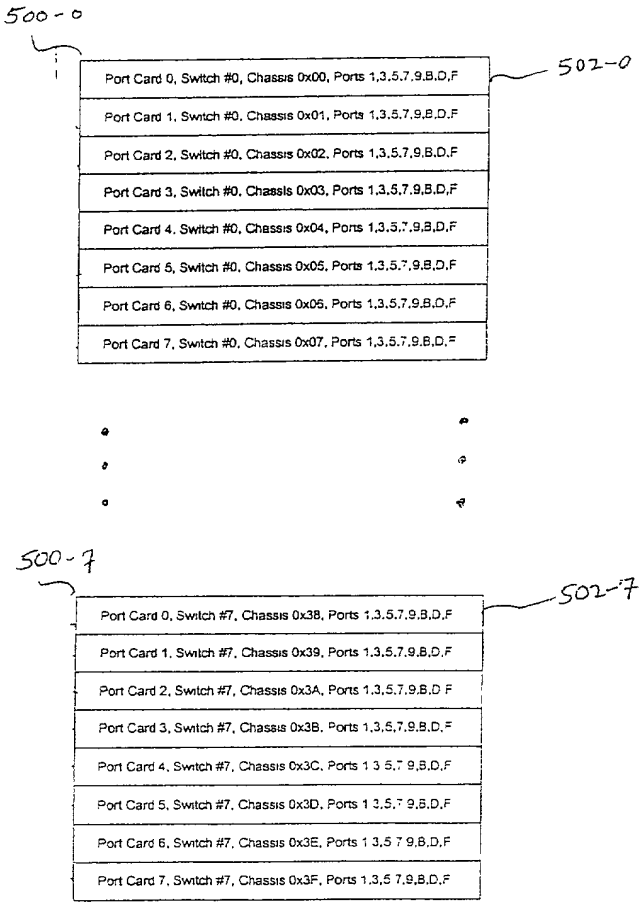
500-0
Port Card 0, Switch #0, Chassis 0x00, Ports 1,3,5,7,9,B,D,F
Port Card 1, Switch #0, Chassis 0x01, Ports 1,3,5,7,9,B,D,F
Port Card 2, Switch #0, Chassis 0x02, Ports 1,3,5,7,9,B,D,F
Port Card 3, Switch #0, Chassis 0x03, Ports 1,3,5,7,9,B,D,F
Port Card 4, Switch #0, Chassis 0x04, Ports 1,3,5,7,9,B,D,F
Port Card 5, Switch #0, Chassis 0x05, Ports 1,3,5,7,9,B,D,F
Port Card 6, Switch #0, Chassis 0x06, Ports 1,3,5,7,9,B,D,F
Port Card 7, Switch #0, Chassis 0x07, Ports 1,3,5,7,9,B,D,F
502-0
500-7
Port Card 0, Switch #7, Chassis 0x38, Ports 1,3,5,7,9,B,D,F
Port Card 1, Switch #7, Chassis 0x39, Ports 1,3,5,7,9,B,D,F
Port Card 2, Switch #7, Chassis 0x3A, Ports 1,3,5,7,9,B,D F
Port Card 3, Switch #7, Chassis 0x3B, Ports 1,3,5,7,9,B,D,F
Port Card 4, Switch #7, Chassis 0x3C, Ports 1 3 5,7 9,B,D,F
Port Card 5, Switch #7, Chassis 0x3D, Ports 1 3,5,7 9,B,D,F
Port Card 6, Switch #7, Chassis 0x3E, Ports 1 3,5 7 9,B,D,F
Port Card 7, Switch #7, Chassis 0x3F, Ports 1,3,5 7,9,B,D,F
502-7

Fig 14

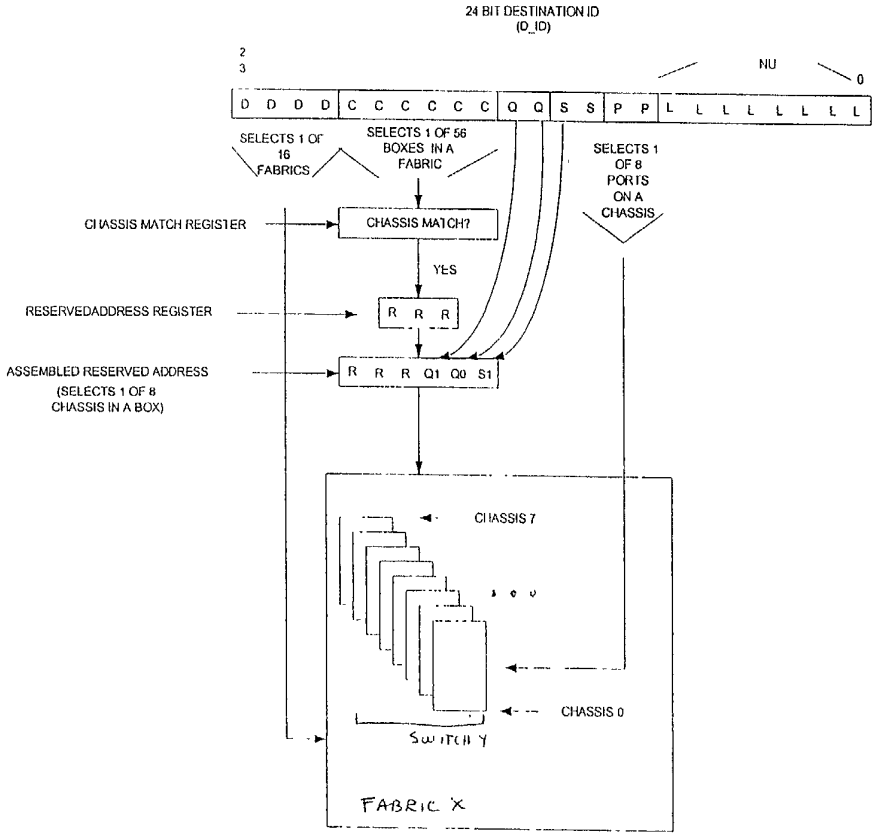
24 BIT DESTINATION ID
(D_ID)
2
3
NU
0
D D D D C C C C C C Q Q S S P P L L L L L L L L
SELECTS 1 OF 16 FABRICS
SELECTS 1 OF 56 BOXES IN A FABRIC
SELECTS 1 OF 8 PORTS ON A CHASSIS
CHASSIS MATCH REGISTER
CHASSIS MATCH?
YES
RESERVEDADDRESS REGISTER
R R R
ASSEMBLED RESERVED ADDRESS
(SELECTS 1 OF 8 CHASSIS IN A BOX)
R R R Q1 Q0 S1
CHASSIS 7
CHASSIS 0
SWITCH Y
FABRIC X

FIG. 15

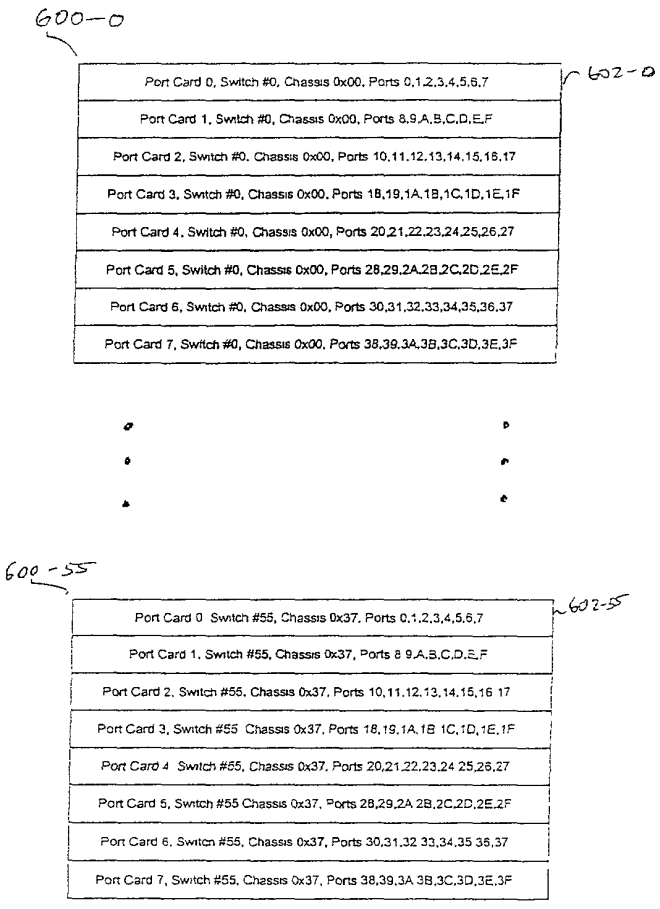
600-0
Port Card 0, Switch #0, Chassis 0x00, Ports 0,1,2,3,4,5,6,7
602-0
Port Card 1, Switch #0, Chassis 0x00, Ports 8,9,A,B,C,D,E,F
Port Card 2, Switch #0, Chassis 0x00, Ports 10,11,12,13,14,15,16,17
Port Card 3, Switch #0, Chassis 0x00, Ports 18,19,1A,1B,1C,1D,1E,1F
Port Card 4, Switch #0, Chassis 0x00, Ports 20,21,22,23,24,25,26,27
Port Card 5, Switch #0, Chassis 0x00, Ports 28,29,2A,2B,2C,2D,2E,2F
Port Card 6, Switch #0, Chassis 0x00, Ports 30,31,32,33,34,35,36,37
Port Card 7, Switch #0, Chassis 0x00, Ports 38,39,3A,3B,3C,3D,3E,3F
600-55
Port Card 0 Switch #55, Chassis 0x37, Ports 0,1,2,3,4,5,6,7
602-55
Port Card 1, Switch #55, Chassis 0x37, Ports 8 9,A,B,C,D,E,F
Port Card 2, Switch #55, Chassis 0x37, Ports 10,11,12,13,14,15,16 17
Port Card 3, Switch #55 Chassis 0x37, Ports 18,19,1A,1B 1C,1D,1E,1F
Port Card 4 Switch #55, Chassis 0x37, Ports 20,21,22,23,24 25,26,27
Port Card 5, Switch #55 Chassis 0x37, Ports 28,29,2A 2B,2C,2D,2E,2F
Port Card 6, Switch #55, Chassis 0x37, Ports 30,31,32 33,34,35 36,37
Port Card 7, Switch #55, Chassis 0x37, Ports 38,39,3A 3B,3C,3D,3E,3F

FIG 16

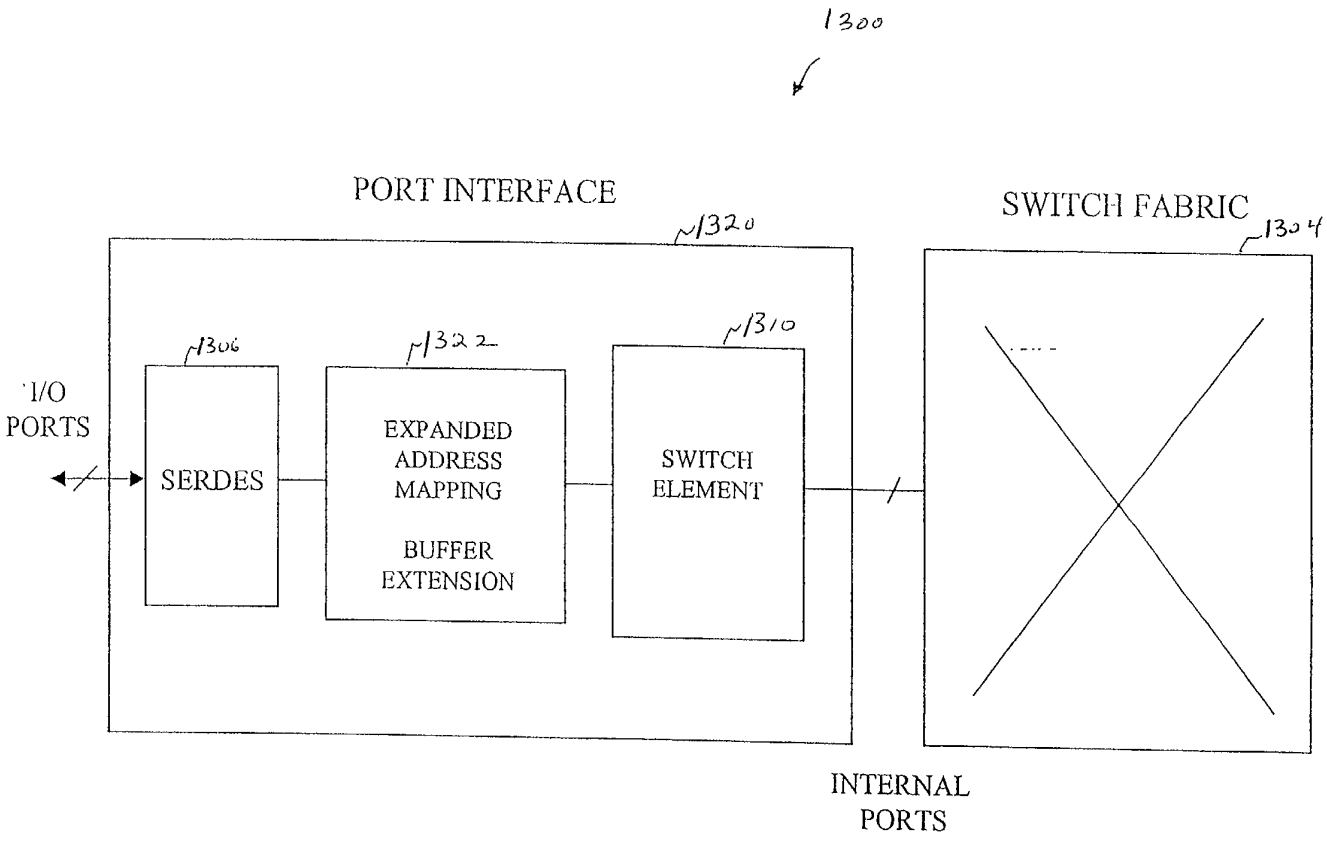
1300
PORT INTERFACE
1320
SWITCH FABRIC
1304
1306
1322
1310
I/O
PORTS
SERDES
EXPANDED
ADDRESS
MAPPING
BUFFER
EXTENSION
SWITCH
ELEMENT
INTERNAL
PORTS

FIG 17

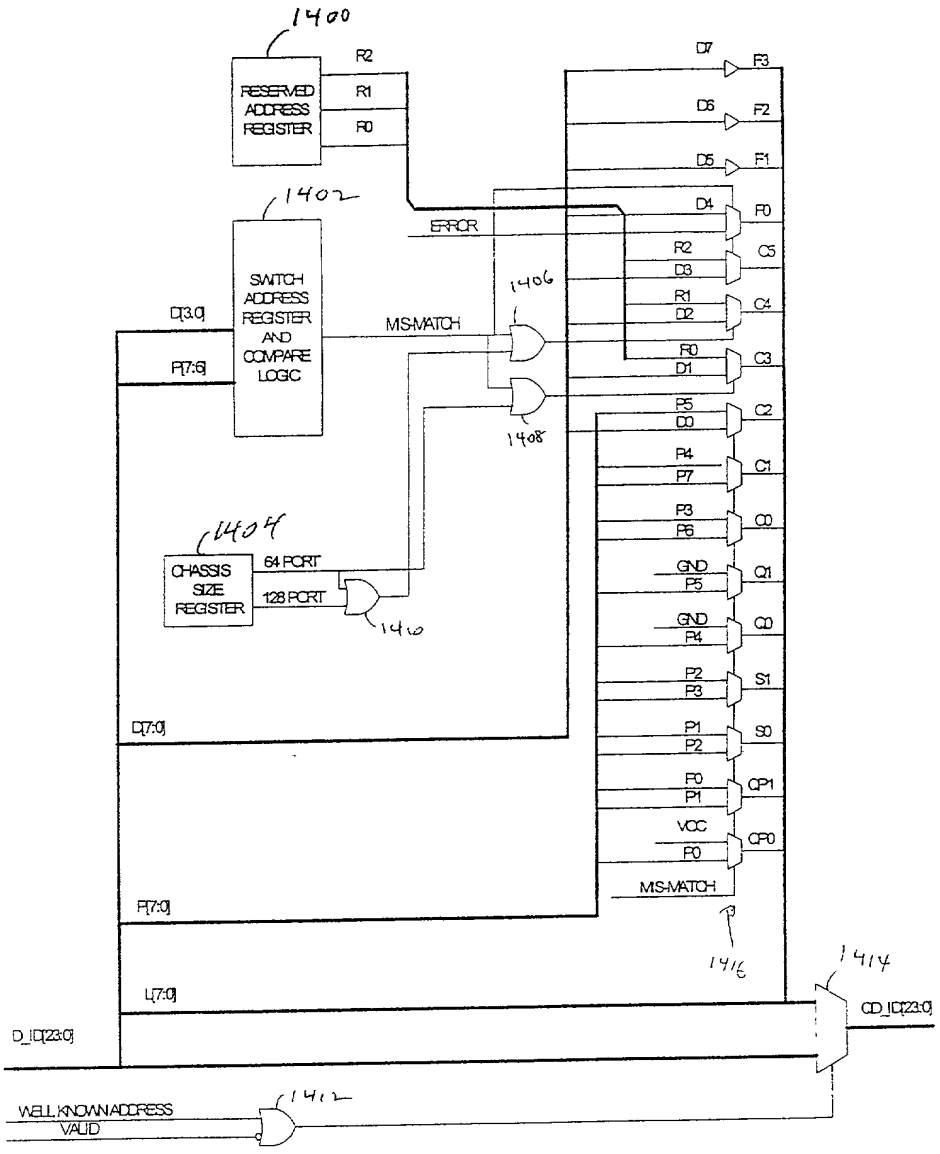
1400
RESERVED ADDRESS REGISTER
R2
R1
R0
1402
SWITCH ADDRESS REGISTER AND COMPARE LOGIC
D[3:0]
P[7:6]
MS-MATCH
ERROR
1406
1408
1404
CHASSIS SIZE REGISTER
64 PORT
128 PORT
1410
D[7:0]
P[7:0]
L[7:0]
D_ID[23:0]
WELL KNOWN ADDRESS VALID
1412
D7
D6
D5
D4
R2
D3
R1
D2
R0
D1
P5
D0
P4
P7
P3
P6
GND
P5
GND
P4
P2
P3
P1
P2
P0
P1
VCC
P0
MS-MATCH
F3
F2
F1
F0
C5
C4
C3
C2
C1
C0
C1
C0
S1
S0
CP1
CP0
1416
1414
CD_ID[23:0]

FIG. 18

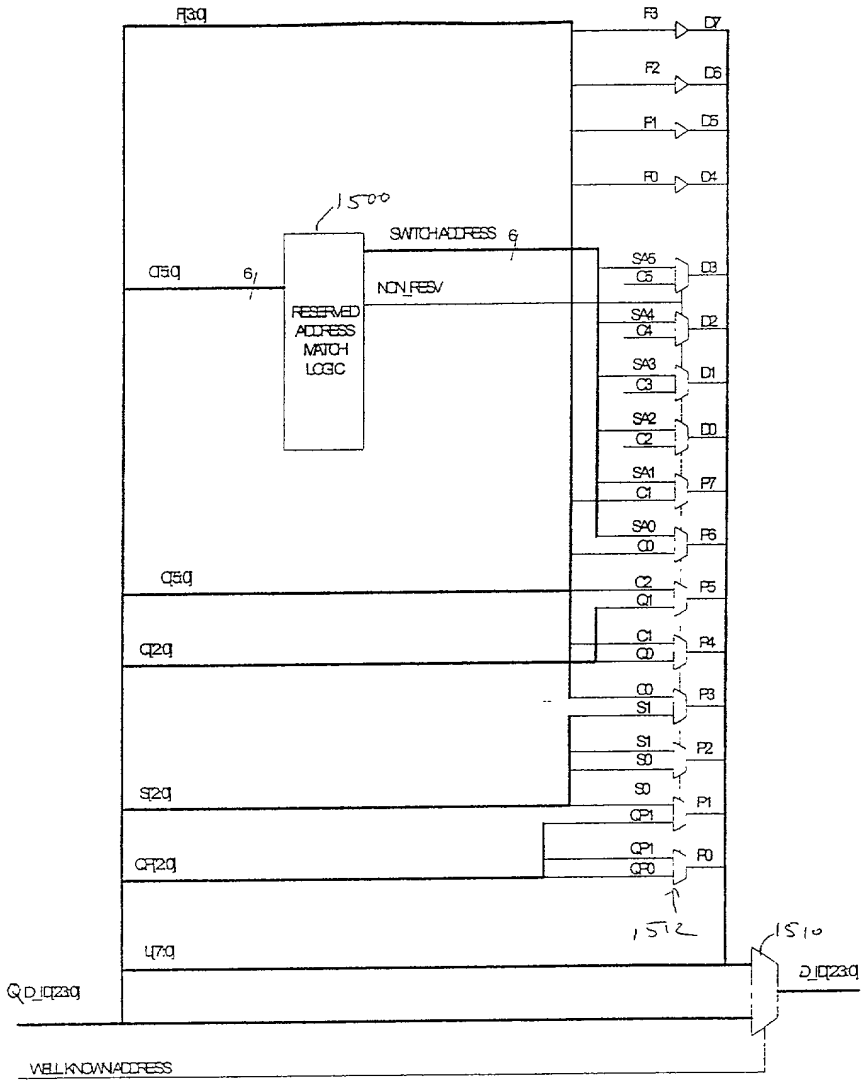
F[3:0]
F3
D7
F2
D6
F1
D5
F0
D4
1500
SWITCHADDRESS
6
C[5:0]
6
NON_RESV
RESERVED ADDRESS MATCH LOGIC
SA5
C5
D3
SA4
C4
D2
SA3
C3
D1
SA2
C2
D0
SA1
C1
P7
SA0
C0
P6
C[5:0]
C2
C1
P5
C[2:0]
C1
C0
P4
C0
S1
P3
S1
S0
P2
S[2:0]
S0
CP1
P1
CP[2:0]
CP1
CP0
P0
1512
1510
U[7:0]
D_IO[23:0]
Q_D_IO[23:0]
WELL_KNOWN_ADDRESS

FIG. 19

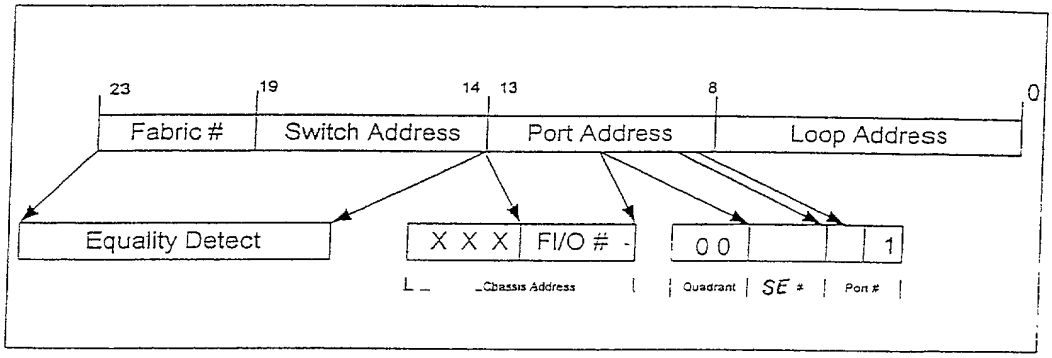
23
19
14
13
8
0
Fabric #
Switch Address
Port Address
Loop Address
Equality Detect
X X X
FI/O #
0 0
1
Chassis Address
Quadrant
SE #
Port #

FIG. 20

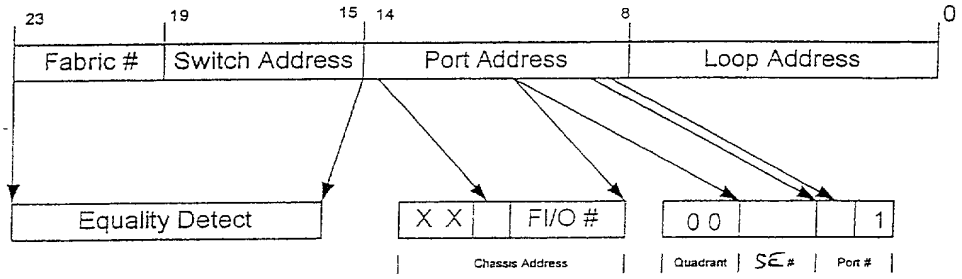
23
19
15
14
8
0
Fabric #
Switch Address
Port Address
Loop Address
Equality Detect
X X
FI/O #
0 0
1
Chassis Address
Quadrant
SE #
Port #

FIG. 21

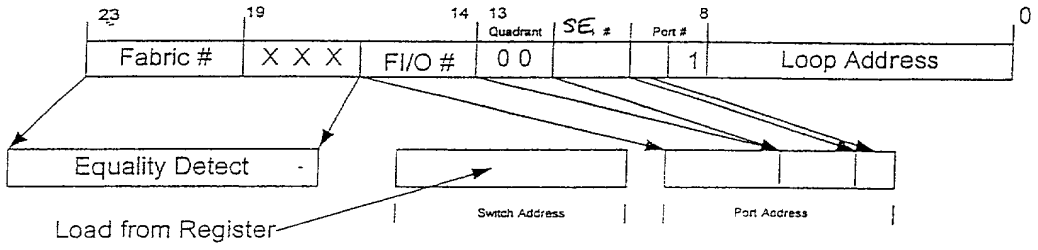
23
19
14
13
Quadrant
SEL #
Port #
8
0
Fabric #
X X X
FI/O #
0 0
1
Loop Address
Equality Detect
Load from Register
Switch Address
Port Address

FIG. 22

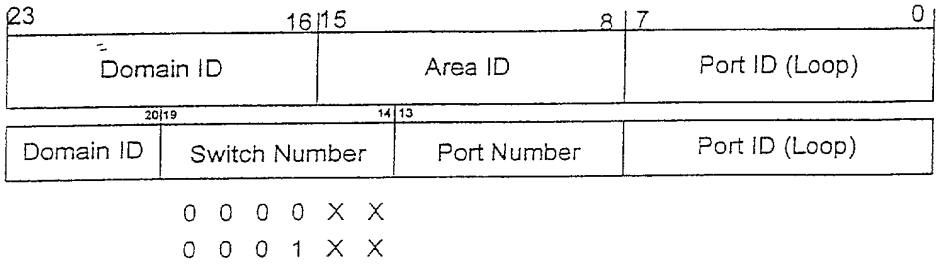
23
16
15
8
7
0
Domain ID
Area ID
Port ID (Loop)
20
19
14
13
Domain ID
Switch Number
Port Number
Port ID (Loop)
0 0 0 0 X X
0 0 0 1 X X

FIG. 23